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EXAMINER	
SHOLEMAN, ABU S	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/568,618	GOLIC, JOVAN	
	Examiner	Art Unit	
	ABU SHOLEMAN	2437	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-82* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-82* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/20/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the request for re-consideration filed on 02/20/2009.

2. Claims 42-82 are presently pending. Claims amended herein are 42, 69 and 77.

Response to Amendment

3. Applicant's arguments, see pages 12-17, filed on 02/20/2009, with respect to the rejection(s) of claim(s) 42-82 under 35 U.S.C § 103(a), have been fully considered but are moot in view of the new ground(s) of rejection .

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 42-68, 69-76, 77-82 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, Claims 42 and 69 have been amended to include the limitation "wherein said transformation circuit transforms said remaining portion of said input block of bits without receiving said first portion of said input block of bits as an input". However, there does not appear to be sufficient written description of this limitation in the specification

as filed. It is noted that any negative limitation must have basis in the original disclosure. Although the specification appears to be silent as to whether there would be any indication of remaining portion of said input block of bits without receiving said first portion of said input block of bits as an input (in particular, it is noted that the term "without receiving said first portion" appears to be absent from the specification entirely), the mere absence of a positive recitation is not basis for an exclusion. See MPEP § 2173.05(i). There does not appear to be sufficient written description of the claim limitations in the application as filed. See MPEP § 2163.04.
Claims not specifically referred to above are rejected due to their dependence on a rejected base claim.

6. Claim 77 has been amended to include the limitation "by inputting said selected k bits into a transformation circuit without also inputting said first portion m of bits into said transformation circuit". However, there does not appear to be sufficient written description of this limitation in the specification as filed. It is noted that any negative limitation must have basis in the original disclosure. Although the specification appears to be silent as to whether there would be any indication of inputting said selected k bits into a transformation circuit without also inputting said first portion m of bits into said transformation circuit without also inputting said first portion m of bits into said transformation circuit (in particular, it is noted that the term "without also inputting said first portion m of bits into said transformation circuit), the mere absence of a positive

recitation is not basis for an exclusion. See MPEP § 2173.05(i). There does not appear to be sufficient written description of the claim limitations in the application as filed. See MPEP § 2163.04.

Claims not specifically referred to above are rejected due to their dependence on a rejected base claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 42-82 are rejected under 35 U.S.C.103(a) as being unpatentable over Viktor et al (Two Methods of Rijndael Implementation in Reconfigurable Hardware)(hereinafter Viktor) in view of Matsui et al (Patent Number: 5261003)(hereinafter Matsui) and further in view of Alfred J. Menezes (Applied cryptography)(hereinafter Menezes).

As per claim 42, Viktor discloses "A combinatorial key-dependent network for encryption / decryption of input digital data of word size N into output digita data of the same word size " as (page 84, Fig 5, One round of the cipher is implemented as a mixture of combinatorial function of 128 bits of input plaintext and 128 bits of output cipher text), “comprising at least two layers” as (page 84, Fig 5, combinatorial function layer and round layer), “ each layer comprising at least an elementary building block” as (page 84, line 1-4, Internal data block is processed in 64 bit sub-blocks), “ each building block operating on an input block of bits having a word size n+m smaller than or equal to said word size N. for generating an output block of bits " as (page 84, Fig 5, combinatorial function block using input bits of 128 bits of plaintext that generates output of the cipher text of 128bits), but Viktor fails to disclose "a multiplexer circuit , receiving on a control input a first portion m of said block of bits, for selecting k out of 2 ^{m}K key bits on a k-bit output of said multiplexer circuit, said first portion of bits being transformed intact to an output of said building block ; and a transformation circuit, for transforming a remaining portion n of said input block of bits into transformed bits according to a reversible transformation chosen, by means of said selected k bits, among a plurality of reversible transformations implemented in said transformation circuit. wherein said transformation circuit transforms said remaining portion of said input block of bits without receiving said first portion of said input block of bits as an input".

However, Matsui discloses “a multiplexer circuit , receiving on a control input a first portion m of said block of bits (column 6, lines 4-6, and Fig 1, input step receiving more significant 4 bytes into block), for selecting k out of $2^{m}K$ key bits on a k-bit output of said multiplexer circuit (column 6, lines 24-26, the selectors are prepared to select the processing block(i.e. block of bits)), said first portion of bits being transformed intact to an output of said building block” as (column 5-6 , and Fig 1, numeral 33 designate an input step for inputting data to be scrambled and output to the next step); and " a transformation circuit, for transforming a remaining portion n of said input block of bits into transformed bits according to a reversible transformation chosen (column 6, lines 5-7, the less significant 4 bytes are input to the processing block 9), by means of said selected k bits (column 6, lines 8-9, the address calculating circuit through the selector 24), among a plurality of reversible transformations implemented in said transformation circuit" as (column 6, lines 56-60, and Fig 1, a plurality of a scramble function f is implement in the input step).

Viktor and Matsui are analogous art because they are from the same field of endeavor of data block scrambling.

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Viktor by including using divided text in the selector (inputting plaintext and key into the multiplexer) and the selector is generating a key that is scrambled with the remaining of the text and scrambling the text that taught by Matsui because it would provide a processing block

by varying the extended cipher keys or the scramble functions depending on an input plaintext to improve random rate and security (column 3, line 58-65).

The combination of Viktor and Matsui fails to teach “wherein said transformation circuit transforms said remaining portion of said input block of bits without receiving said first portion of said input block of bits as an input”.

However, Menezes discloses “wherein said transformation circuit transforms said remaining portion of said input block of bits without receiving said first portion of said input block of bits as an input" as (page 251, and 7.81 , Figure 7.9(b), successive rounds of a Feistel cipher operate on alternating halves of the ciphertext, while other remains constant).

Therefore, It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to modify the teaching of Viktor in view of Matsui by including scrambling one portion keeping other portions constant that is taught by Menezes because it would provide a higher level of security for data processing system.

As per claim 43, Viktor discloses “wherein adjacent layers are connected by means of a fixed bit permutation block" as (page 78-79, section 2.1, line 11-17, byteRotation (permutation) connected to Multiplexer which is in the adjacent layer in the combinatorial circuit, Galois filed is fixed bit of data).

As per claim 44, Viktor discloses “comprising a plurality of fixed bit permutation blocks of the same type" as (page 84, line 1-2, Internal data block is processed in 64 bit

or 32 bit sub-blocks in subsequent clock cycles, so permutation blocks are same type of data).

As per claim 45, Viktor discloses "comprising at least two different types of fixed bit permutation blocks" as (page 84, line 1-2, Internal data block is processed in 64 bit or 32 bit sub-blocks in subsequent clock cycles).

As per claim 46, Viktor discloses " wherein bits in said first portion of said block of bits are used, in a next layer , as bits to be transformed" as (page 84, Fig1, a block of plaintext bits are coming into XORed from byteRotation, then it is XORed with Key to generated a transformed bits of Cipher text).

As per claim 47, Viktor discloses "wherein, for each building block, said first portion of said block of bits are extracted from at least two building blocks in a preceding layer, provided that m>=2" as (page 84, line 1-3, Embedded memory block sharing the data from internal block , the 128-bit cipher state, which is processed in 64(32) bit sub-blocks in 2^4 where is m that is the data portion , so m is m=4 in here, bit sub-blocks can be in 32(16) ,16(8) , 8(4) bit sub-blocks 2^2 where is m =2).

As per claim 48, Viktor discloses " wherein , for each building block, said second portion of said block of bits are extracted from a least two building blocks in a preceding layer, provided that n>=2" as (page 84, line 1-3, Embedded memory block sharing the data from internal block , the 128-bit cipher state, which is processed in 64(32) bit sub-blocks in 2^4 where is n that is the data portion , so n is n=4 in here, bit sub-blocks can be in 32(16) ,16(8) , 8(4) bit sub-blocks 2^2 where is n =2).

As per claim 49, Viktor discloses “wherein each layer comprises at least two building blocks” as (page 79, Fig 1, There are two blocks in this cipher layer one is plaintext and other one is ciphertext).

As per claim 50, Viktor discloses “wherein said reversible transformations are such that each output bit of said transformed bits is a non-linear function of said first portion of said block of bits and of said k key bits, with the algebraic normal form containing at least one binary product involving both said first portion of said block of bits and said key bits" as (page 79, line 19-22, Inverse byte substitution is the non-linear step for reversible transformation).

As per claim 51, Viktor discloses “wherein said reversible transformation satisfy a criterion that the uncertainty of n input bits provided by uniformly random k key bits when the output n bits are known is equal to n bits" as (page 79, Fig 1, line 21-23, where is 128 bits = n bits coming into round key ki after invByteSubstitution and after round transformation the output is same as input).

As per claim 52, Viktor discloses “wherein said multiplexer circuit comprises as lookup table whose content is defined by the key” as (page 79 , line 18-21, In the table-lookup implementation, it is essential only non-linear step in the transformation round that has a round key).

As per claim 53, Viktor discloses " wherein said transformation circuit comprises XOR gates and controlled switches" as (page 84, Fig 5, the first step of this combinatorial circuit compose of XOR gates , there are plaintext and controlled switches come into XOR gates)

As per claim 54, Viktor discloses " wherein each XOR gate has two input bits and one output bit. one of the two input bits being a key bit, and each controlled switch has two input bits, two output bits and one control bit that determines if the input bits are swapped or not, said control bit being a key bit" as (page 84, Fig 5, XOR gate has two input. one is K key bits and other one is ByteRotation bits).

As per claim 55, Viktor discloses "wherein said multiplexer circuit has two control bits, four 3-bit inputs and one 3-bit output, and said transformation circuit comprises two XOR gates and one controlled switch" as (page 84, Fig 5, Multiplexer circuit has two controllers fist one is control key ki and 2^{nd} one is MixColumn controlled key it could be any number of bit combination according to input bit).

As per claim 56, Viktor discloses " wherein the three bits of said 3-bit output are connected respectively to a first input bit of each XOR gate and to the control bit of said controlled switch" as (page 84, Fig 5, Any number of cipher text output is connected to XORed input bit and contorlled key at round).

As per claim 57, Viktor discloses " wherein a second input bit of each XOR gate is connected to a bit of said second portion of said block of bits" as (page 84, Fig 5, Input bit into XOR gate into is the part of input bit of ByteRotation block).

As per claim 58, Viktor discloses " wherein the output bits of said XOR gates are connected to the two input bits of said controlled switch" as (page 84, Fig 5, Cipher text bit are connected to XOR gates that connected to any number of bits of ByteRotation).

As per claim 59, Viktor discloses " wherein the two output bits of said controlled switch generate the transformed bits of said transformation circuit" as (page 84, Fig 5, Cipher text can be any number of output bits from the transformation circuit XOR).

As per claim 60, Viktor in view of Matsui discloses "the network according to claim 42", but fails to expressly disclose "comprising a plurality of building blocks of the same type".

However, Matsui discloses, disclose "comprising a plurality of building blocks of the same type" as (column 5, Fig 1, line 50-53, a plurality of processing blocks 9 has the same type of block).

As per claim 61, Matsui discloses “comprising at least two different types of building blocks” as (column 5, Fig 1, line 50-55, block 9 has two different types of blocks data , one is more significant bits and other is the extended keys block).

As per claim 62, Viktor discloses " wherein adjacent layers are connected by means of a block implementing a reversible liner function" as (page 79, Fig 1, InvMixColumn function is implemented as a reversible liner function).

As per claim 63, Viktor discloses “ wherein two additional input and output keys of word size N are bitwise XORed respectively with said input digital data and with said output digital data” as (page 84, Fig 1, K1 input and MaxColumn output of same input bits are XORed)

As per claim 64, Viktor discloses " wherein said key bits in each layer, having bit size k', are generated from a smaller number of secret key bits, having bit size K, by means of a key expansion algorithm" as (page 80, Fig2, The key expansion algorithm uses bit-wise additions module bit values obtained from round addition).

As per claim 65, Viktor discloses “ wherein said k secret key bits are first expanded by means of liner transformation into k' key bits, using a linear code so that any subset of k'' expanded key bits are linearly independent , where $k'' <= k$ " as (page

79, Fig1, MixColumn is a liner transformation of bits those bits are XORed with the key).

As per claim 66, Viktor discloses " wherein said expanded key having bit size of k' is used as an input to a further combinatorial key-dependent network of block size k ' which is parameterized by a fixed randomly generated key satisfying the condition that every multiplexer implements balanced binary lookup tables" as (page 84, Fig 5, Multiplexer implements an expanded key in the combinatorial function from the lookup tables).

As per claim 67, Viktor discloses " wherein the K" bits produced after every two layers of said further combinatorial key-dependent network are used as said key bits from the multiplexer circuits within the layers of the combinatorial network" as (page 79, line , 5-7, Rounds key K are derived from the key schedule in the combinatorial function).

As per claim 68, Viktor discloses " wherein said further combinatorial key-dependent network comprises a plurality of layers, each layer comprising a plurality of simplified building blocks" as (page 84, Fig 5, combinatorial function is the one building blocks), "a multiplexer having one input receiving one control bit which is passed to the output intact, for selecting one out of two key bits on a one bit output" as (page 84, Fig 5, 128 bits data inputting in Multiplexer and same outputting cipher text); and " a

controlled switch having two input bits, two output bits and one control bit connected to the output of said multiplexer, said control bit determining if said two input bits are swapped or not" as (page 84, Fig 5, input bits and key bits are connected to Multiplexer output bit).

As per claim 81, Viktor discloses " A data processing device comprising a central processing unit , volatile or non-volatile memory, and at least a data, instruction or address bus" as (page 84, Fig 5, Cipher data processing unit of combinatorial bus or circuit), "comprising at least a combinatorial key-dependent network according to any one of claims 42 to 68" as (page 84, Fig 5, a combinatorial function) , "for encryption /decryption of digital data on said data, instruction , or address bus and /or into said memories" as (page 79, Fig 1, structure of encryption and decryption layer).

As per claim 82, Viktor discloses " A multimedia device for storing and playing copyright digital data comprising at least a combinatorial key-dependent network according to any one of claims 42 to 68" as (page 84, Fig 5, A combinatorial function that does data encryption for copyright), "for encryption /decryption of said copyright digital data" as (page 79, Fig 1, structure of encryption and decryption layer).

As per claim 69, this claim is directed to a block for secret-key controlled cryptographic functions and contains limitations that are substantially similar to those recited in claim 1 above, and accordingly is rejected for similar reasons.

As per claim 70, Viktor discloses “Where in said transformation circuit comprises XOR gates and controlled switches" as (page 84, Fig 5, ByteRotation bits with key XORed in transformation circuit).

As per claim 71, Viktor discloses “wherein each XOR gate has two input bits and one output bit. one of the two input bits being a key bit, and each controlled switch has two input bits, two output bits and one control bit that determines if the input bits are swapped or not, said control bit being a key bit" as (page 84, Fig 5, XOR gate has two input. one is K key bits and other one is ByteRotation bits).

As per claim 72, Viktor discloses “ wherein said multiplexer circuit has two control bits, four 3-bit inputs and one 3-bit output, and said transformation circuit comprises two XOR gates and one controlled switch" as (page 84, Fig 5, Multiplexer circuit has two controllers fist one is control key ki and 2^{nd} one is MixColumn controlled key it could be any number of bit combination according to input bit).

As per claim 73, Viktor discloses " wherein the three bits of said 3-bit output are connected respectively to a first input bit of each XOR gate and to the control bit of said controlled switch" as (page 84, Fig 5, Any number of cipher text output is connected to XORed input bit and contorlled key at round).

As per claim 74, Viktor discloses " wherein a second input bit of each XOR gate is connected to a bit of said second portion of said block of bits" as (page 84, Fig 5, Input bit into XOR gate into is the part of input bit of ByteRotation block).

As per claim 75, Viktor discloses " wherein the output bits of said XOR gates are connected to the two input bits of said controlled switch" as (page 84, Fig 5, Cipher text bit are connected to XOR gates that connected to any number of bits of ByteRotation).

As per claim 76, Viktor discloses " wherein the two output bits of said controlled switch generate the transformed bits of said transformation circuit" as (page 84, Fig 5, Cipher text can be any number of output bits from the transformation circuit XOR).

As per claim 77, this claim is directed to a block for secret-key controlled cryptographic functions and contains limitations that are substantially similar to those recited in claim 1 above, and accordingly is rejected for similar reasons.

As per claim 78, Viktor discloses" where said step b) is reiterated on a block of bits comprising said first and second portions of previously transformed bits"as (page 84, Fig 5, After MixColumn, 128 bits is combining with previously transformed bits).

As per claim 79, Viktor discloses " wherein , before each reiteration of step b), a fixed bit permutation is applied to said previously transformed bits" as (page 78-79, section 2.1, line 11-17, byteRotation (permutation) connected to Multiplexer which is in the adjacent layer in the combinatorial circuit, Galois filed is fixed bit of data).

As per claim 80, Viktor discloses " wherein, before each reiteration of step b), a reversible linear function is applied to said previously transformed bits" as (page 81, Fig 4, InvMixColumn is linear transformation that is apply after cipher text transformation that is said previously transformed).

Examiner Notes

9. Examiner cites particular columns and line numbers in the references as applied to the claims below for the convenience of the applicant. Although the specified citations

are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abu Sholeman whose telephone number is (571)270-7314. The examiner can normally be reached on Monday through Thursday 9:00 AM - 6:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 15, 2009

Abu Sholeman
Examiner
Art unit 2437

/Emmanuel L. Moise/
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